REMARKS

The Office Action mailed July 2, 2002, has been received and reviewed. Claims 1 through 29 are currently pending in the application. Claims 21 through 29 have been withdrawn from consideration as being drawn to a non-elected invention. Claims 1 through 20 stand rejected. Applicants respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,147,413 to Farnworth in View of U.S. Patent No. 5,894,107 to Lee et al.

Claims 1 through 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Farnworth (U.S. Patent No. 6,147,413) in view of Lee et al. (U.S. Patent No. 5,894,107). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness type rejection of claims 1 through 20 is improper because it fails to establish a *prima facie* case of obviousness.

Turning to the cited references, Farnworth describes a method of forming conductive bumps on a die for flip chip type attachment using simplified masking steps. In the method, a first polyamide passivation layer 1006 is applied to a wafer active surface 1010 by spin coating (col. 4, lines 3-10). A via 1008 is etched through passivation layer 1006 to expose bond pad 1002 (col. 4, lines 27-32). A conductive layer 1012 is then deposited over passivation layer 1006 and masked and etched to form repattern trace 1016 which extends to an alternative bond pad

location (col. 4, lines 39-44). A second passivation layer 1018 is spun-on over repattern trace 1016, and a via 1026 is formed therein to connect a solder ball 1032 to the alternative bond pad location of repattern trace 1016 (col. 4, line 45 - col. 5, line 40).

Lee et al. teaches a prior art chip-size package that uses half etched leads 76 to connect to bonding pads 74. (Fig. 1 and cols. 1 and 2). Leads 76 are attached to an active surface of semiconductor chip 72 by adhesive tape 78, and bonding pads 74 are connected to leads 76 with wires 80 (col. 1, line 66 - col. 2, line 1). The assembly is encapsulated with epoxy molding compound 82 such that bonding pads 74 and wires 80 are protected from the external environment, while the thick portions of leads 76 are exposed to the outside (col. 2, lines 1-8).

Applicants respectfully submit there is no suggestion or motivation in the cited references or from the knowledge generally available in the prior art which would lead one of ordinary skill in the art to combine the teachings of Lee et al. with Farnworth in the manner presented in the instant rejection. The Office acknowledges Farnworth does not describe the claimed discrete conductive bond, but suggests that it would be obvious to "modify the conductive trace configuration of Farnworth by employing a lead on chip configuration as taught by Lee to increase the package density and provide better electrical performance." Due to the differences in structure and scale between the repattern traces of Farnworth and the wires of Lee et al., Applicants submit there is no support for this line of reasoning. Adding bond wires to the repattern structure of Farnworth would require an enlarged packaged size to accommodate them within the passivation layer 1018, and therefore would reduce package density. Furthermore, the wires would add length to the conductive pathway between bond pad 1002 and solder ball 1032, which would lower electrical performance rather than improve it.

Even if some motivation could be found for adding bond wires to the structure of Farnworth, there is no reasonable expectation of success for the combination, as the trace formation process used in Farnworth is not compatible with bond wires. As described above, Farnworth uses a series of mask, etch and spin coat steps to form via 1008 and repattern trace 1016 and to cover the trace configuration with passivation layer 1018 (Farnworth at col. 4). It is unclear how these steps could be carried out in the presence of bond wires. At the least, the

process described by Farnworth would require major alterations to provide the proposed combination, rendering it non-obvious.

Moreover, Applicants respectfully submit that Farnworth teaches away from any combination with Lee et al. Farnworth indicates an object of the invention is to simplify or eliminate masking steps in UBM pad forming with repatterning (Abstract and col. 1, lines 14-22). In its present form, the invention described by Farnsworth allows the repattern trace 1016 connecting bond pad 1002 and solder ball 1032 to be formed with a single mask and etch step (col. 4, lines 39-44). In order to include an intermediate bond wire between repattern trace 1016 and bond pad 1002, additional or more complicated masking steps would be required. Further process steps would also be necessary in terms of connecting trace 1016 and bond pad 1002 with a bond wire instead of directly connecting them.

In view of the foregoing, Applicants respectfully submit that the combination of Farnworth with Lee et al. as presented does not establish a prima facie case of obviousness under 35 U.S.C. § 103(a), and respectfully request the rejection of claims 1 through 20 be withdrawn.

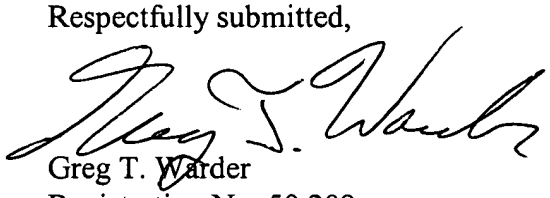
Drawings

Applicants will file corrected formal drawings upon receipt of a Notice of Allowance and Issue Fee Due in the application.

CONCLUSION

Claims 1 through 20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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Date: October 2, 2002

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